Notice of Allowability	Application No.	Applicant(s)	
	10/765,956	FUNAMOTO, KENJI	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendments filed Jaunary 31, 2006*.

2. ☒ The allowed claim(s) is/are *1-3 and 5-19*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-3 and 5-19 are pending and have been examined.

2. Claims 1-3 and 5-19 are allowed.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance:

The Examiner has done a thorough search and found no prior art of record that provides suitable motivation for one of ordinary skill in the art to be combine the teachings of the prior art and construct the claimed invention. The individual limitations of the independent claims are separately taught or suggested by the prior art but absent a suitable motivation to combine the teachings of the prior art the instant application is considered allowable over the prior art of record. The Examiner will now discuss the individual limitations of representative independent claim 1 and how each limitation along has been suggested by the prior art. Since independent claims 1, 18 and 19 contain substantially equivalent limitations they will all be addressed through the Examiner's interpretation of independent claim 1.

Regarding a data memory to and from which image data is input and output via a data bus for a data memory the Examiner had previously rejected the pending claims over Muramatsu et al. (US006384832B1) who discloses in column 4, line 65 through column 5, line 2 "The data transfer part 20 accesses the shared memory 2 so that the function selected by the high priority function part 30 can be processed, and then reads a set of **image data** out of the shared memory

2..." As apparent from the cited passage a data memory for storing image data is well known in the art.

Regarding a plurality of buffer circuits for inputting and outputting image data to and from said data memory via a first data bus that has a bus width the same as that of the data bus for said data memory and that is electrically connected to the data bus for said data memory, and inputting and outputting image data to and from a data processing circuit via a second data bus having a bus width smaller than that of the data bus for said data memory, the Examiner will now address the individual components of this limitation separately. A plurality of buffer circuits for inputting and outputting image data from a data memory is well known in the art as evidenced by Okumura et al. (US005974493A) (Fig. 2 simply shows buffers between a memory bus and a processor bus), Schinnerer (US006894692B2) (column 1, lines 39-60 describe how triple buffering image data is well known in the art) and Wakasu (US005513301A) (Fig. 11 and 12, column 1, line 46 – column 2, line 64 describes double and triple buffering is well known in the art for compressing and decompressing video streams) among others. A memory bus having a width greater then the width of a data processing circuit bus is well known in the art as evidenced by Gelke et al. (US 2002/0011607A1) in paragraphs [0032-0033] that state "flash bus 3 has a bus width which is a multiple of the microprocessor's width to compensate for the flash memory's limited access performance."

Regarding an arbitration circuit, which is connected between the data processing circuit and said plurality of buffer circuits, for controlling the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different buffer circuits in a common time period. Wakasu (US005513301A) teaches a double buffer

circuit for storing and reading temporarily stored image data during the process of compression (column 5, lines 5-63). In Wakasu, one buffer is read to while a second buffer is being written to. This process is commonly known in the art as "double buffering" "ping-pong buffering" or alternatively by the process known as "buffer swapping." Wakasu however lacks an arbitration circuit connected between a data processing circuit (i.e. "host computer" column 3, line 65) and instead discloses a memory controller (Fig. 1, item 9) that controls the output of the buffers (Fig. 1, items 7 and 8). While this shows the memory controller connected between the buffer circuits and the data processing circuit (i.e. the "computer bus") it does not show the buffer circuits are connected to a 1st bus prior to the arbitration circuit. As such Wakasu does not teach and/or fairly suggest each and every limitation of the claimed invention. Furthermore the Digital Video Signal of Wakasu is not described to come from a data memory (as claimed in the instant application) but rather comes directly from a video stream. Schinnerer (US006894692B2) teaches system and method for synchronizing video data streams. In Schinnerer a double buffer (Fig. 2, items 46 and 47) is used to receive and output video data in a common time period (column 4, line 7-24, column 5, lines 12-20 and column 6, lines 44-53). The buffering logic (Fig. 2, items 50) are in controller of the buffer circuit such that one buffer is receiving data while the other is sending data. While the buffer logic is shown to encompass the buffer circuits and not shown to be connected between the buffer circuits and the data processing circuit attached to the bus 35 (Fig. 1 and 2), one of ordinary skill in the art would understand the prior art of Schinnerer and the claimed arbitration circuit to be functionally equivalent because they both accomplish the same goal of "controlling the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different

buffer circuits in a common time period." However, Schinnerer much like Wakasu fails to teach and/or fairly suggest the video data is retrieved from a data memory but instead the specification of Schinnerer appears to disclose the video signal is created dynamically and not retrieved from a data memory.

In light of the foregoing comments pending claims 1-3 and 5-19 are allowable over the prior art of record. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

RMS

PAUL R. MYERS
PRIMARY EXAMINER